Atty Docket No. AM524R1/T28900

PTO FAX NO.: 1-703-305-6357

ATTENTION: Examiner Marianne Padgett
Group Art Unit 1762

OFFICIAL COMMUNICATION

FOR THE PERSONAL ATTENTION OF

EXAMINER MARIANNE PADGETT

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following: Communication; copy of Office Action mailed October 6, 1997 relating to U.S. Appl. No. 08/691,983; copy of Figures 1C, 2 and 3 relating to U.S. Appl. No. 08/691,983; copy of claimed as filed in U.S. Appl. No. 08/691,983; in re Application of Katsuyuki Musaka et al.; Appl. No. 09/187,551; filed November 5, 1998; for METHOD FOR FORMING A THIN FILM FOR A SEMICONDUCTOR DEVICE is being facsimile transmitted to the Patent and Trademark Office on the date shown below.

Number of pages being transmitted, including this page: 23

Dated: May 14, 1999

Kristina Alvarez

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PA 192258 v1

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Washington, D.C. 20231

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NO.
			850/P00

COMPUTER ENTERED
OCT 16 1997

GAILE BAILEY

EXAMINER

ART UNIT	PAPER NUMBER
	5

PATENT COUNSEL
APPLIED MATERIALS INC
LEGAL AFFAIRS DEPT
3050 BOWERS AVENUE
SANTA CLARA CA 95054

OFC 1.6
Dead 46

DATE MAILED:

This is a communication from the examiner in charge of your application.
COMMISSIONER OF PATENTS AND TRADEMARKS

OFFICE ACTION SUMMARY

☐ Responsive to communication(s) filed on 5/9/97

☐ This action is FINAL.

☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 D.C. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) 1-21 is/are pending in the application.

Of the above, claim(s) 17-21 is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 1-16 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

☒ U.S. DOCKET ☐ FOREIGN DOCKET

Attachment(s)

☒ Notice of Reference Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 4

☐ Interview Summary, PTO-413

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

– SEE OFFICE ACTION ON THE FOLLOWING PAGES –

PTOL-326 (Rev. 10/96)

* U.S. GPO: 1998-405-280 40029

I hereby certify that this correspondence is being sent by facsimile transmission to:

Examiner Marianne Padgett
at Fax No.: 1-703-305-6357

On 5/14/99
TOWNSEND and TOWNSEND and CREW LLP
By:

PATENT

Attorney Docket No.: AM524R1/T28900

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Examiner: Marianne Padgett
KATSUYUKI MUSAKA et al.	Art Unit: 1762
Application No.: 09/187,551	COMMUNICATION
Filed: November 5, 1998	
For: METHOD FOR FORMING A THIN FILM FOR A SEMICONDUCTOR DEVICE	

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to your recent request, attached are a copies the following documents you requested that relate to U.S. Application No. 08/691,983, filed August 2, 1996.

1) Office Action mailed October 6, 1997;

2) copy of Figures 1C, 2 and 3; and

3) a copy of the claims as filed.

If the Examiner requires further information, please do not hesitate to contact the me at (650) 326-2400.

Respectfully submitted,

William L. Shaffer
Reg. No. 37,234

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FORM PTO-892 (REV. 3-93) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

NOTICE OF REFERENCES CITED

SERIAL NO.	GROUP ART UNIT	ATTACHMENT TO PAPER NUMBER
08/69,983	1112	5

APPLICANT(S): Nowak etal

U.S. PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE IF APPROPRIATE
	A	5571571	11/5/96	Musaka et al	427	575	6/14/94
	B	5279865	1/94	Chekai etal	427	579	
	C						
	D						
	E						
	F						
	G						
	H						
	I						
	J						
	K						

FOREIGN PATENT DOCUMENTS

*		DOCUMENT NO.	DATE	COUNTRY	NAME	CLASS	SUB-CLASS	PERTINENT SHTS. DWG.	PERTINENT PP. SPEC.
	L								
	M								
	N								
	O								
	P								
	Q								

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)

R	
S	
T	
U	

EXAMINER: [signature] DATE: 9/20/97

* A copy of this reference is not being furnished with this office action. (See Manual of Patent Examining Procedure, section 707.05 (a).)

(1) Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-16, drawn to a method of depositing a layer with an intrinsic stress level in a substrate from Si,0 and halogen containing source gas in a plasma, classified in class 427, subclass 579.

II. Claim 17, drawn to an integrated circuit with an insulating layer of fluorosilicate glass (FSG) with a stress level, classified in class 428 or 257, subclass 426+ or 506, respectively.

III. Claims 18-21 are, drawn to a plasma apparatus with a controller for the gas delivery system, classified in class 118, subclass 697 or 723I.

(2) The inventions are distinct, each from the other because:

Inventions group I and group II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the particular gas used is not apart of the apparatus and specific instruction in a memory are method limitations that do not further limit the structure of the apparatus, hence different deposition gases may be used in the apparatus.

(4) Inventions group I and group II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP

§ 806.05(f)). In the instant case the insulating layer of FSG may be deposited via different plasma apparatus than the RF inductively coupled plasma process claimed, such as multifrequency plasmas, and may be used in products other than integrated circuits.

(5) Inventions group III and group II are related as apparatus and product made. The inventions in this relationship are distinct if either or both of the following can be shown: (1) that the apparatus as claimed is not an obvious apparatus for making the product and the apparatus can be used for making a different product or (2) that the product as claimed can be made by another and materially different apparatus (MPEP § 806.05(g)). In this case the product may be made in different apparatus as associated with the different processes discussed above, and the apparatus may be used to deposit layers of different materials.

(6) Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classifications, their divergent subject matter and their different required searches, restriction for examination purposes as indicated is proper.

(7) During a telephone conversation with William Shaffer on 1/7 and 9/96 a provisional election was made with traverse to prosecute the invention of group I method, claims 1-16. Affirmation of this election must be made by applicant in responding to this Office action. Claims 17-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

(8) Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the

currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a diligently-filed petition under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(h).

(9) Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 8 and 11, in the preambles "the steps of" lacks proper antecedent basis because applicants are introducing new steps, hence "the" should be deleted.

Use of abbreviations, such as TEFS or TEOS or HDP CVD, without first writing the limitation out in full, is improper in claim language.

In claim 8, when step(e) is preformed is not stated, hence can be after all of the plurality of substrates are coated, so there are none left to follow for step (f). In both lines 8 and 12 "a halogen-doped silicon oxide film" either needs to use an article showing antecedent basis or needs differentiation. Likewise, for "a subsequently processed substrate" in line 13.

Use of relative terms is vague and indefinite if they lack clear metes and bounds. See "too high" and "too low" in lines 7 and 11, respectively. If the "H" in HDP stands for high, it too will be relative.

In claim 16, line 2 "a rate" uses the incorrect article for an already introduced term. Also, the basis for calculating the percentages needs to be defined since vol. or weight or moles will give different values. Number of F in a molecule may also be significant, as will the specific sources reactivity.

10. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

(11) Claims 1-7 and 9 are rejected under 35 U.S.C. 102(e) as being clearly anticipated by Musaka et al. See Abstract; Fig 3-6 for plasma apparatus; Fig. 10 ([F] in atomic % VS. C_2F_2 flow (~~80CM~~ sccm)); Fig. 11 ([F] in atomic % VS. dielectric constant) with values from 3.2-4.2; Fig. 13 (stress vs. C_2F_2 flow in SCCM) ranging from about -1.25×10^9 Dyne/cm^2 to about $.5\times10^9$ dyne/cm^2; col. 4, lines 54-68 for use of TEOS and fluorine sources including CF_4, C_2F_6, CHF_3, F_2, etc. for the plasma and some ratio relationships; col. 6, lines 15-45; col. 7, line 46-65; col. 8, lines 20- col. 9, lines 37 for various examples and relationships, esp. col 8, lines 58 to 65; col. 9, lines 7-11 and following discussion of the graphs. Note that the graphs are data bases of previously deposited films.

(12) Claims 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Musaka et al.

Musaka et al do not discuss using their technique in an assembly line (ie. repeated like treatments of successive substrates), nor their data to adjust parameters in that assembly line,

however it would have been obvious to one of ordinary skill in the art that to use Musaka et al's process industrially, that the deposition, ie steps a-c, would be repeatedly preformed and that any process should involve quality control procedures to ensure that ones desired properties, which are stress and dielectric constant for Musaka et al. Therefore, it would have been further obvious to measure intrinsic stress of the product of the assembly line as a check on the deposition, and to adjust the flow rate of the halogen gas according to previous measurements as illustrated in Fig. 13, because this would have been the logical way to correct deviations, given Musaka et al's data.

(13) Claims 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Musaka et al as applied to claims 1-15 above, and further in view of Nishiyama et al.

Musaka et al teaches use of a variety of plasma apparatus, exemplified by parallel plate RF reactor a microwave ECR plasma reactor (Figures 3-6), but does not teach the type that applies RF power to a coil, nor the plasma densities of those employed. Nishiyama et al who teaches RF parallel plate plasmas for analogous depositions (Fig. 1, 4-7, 9, 14-16 and 20; and Examples 1, 3, 6 and 8) that produce fluorinated silica deposits, also teaches a plasma CVD apparatus with an RF antenna (ie coil) that produces a plasma density of $3.5 \times 10^{11}/cm^3$ used for like depositions (Fig. 17-18 and Ex. 7 on col. 13-14). Where TEOS + O_2+NF_3 are given as a specific example and CF_4,C_2F_6,$FSi(OC_2H_5)_3$, $F_2Si(OC_2H_5)_2$ are taught as alternative to the nitrogen fluoride. It would have been obvious to one of ordinary skill in the art that Nishiyama's high density plasma apparatus that uses an RF antenna and that produces SiO_2 fluorinated films with low dielectric constants would have been expected to produce

analogously low stress values as in Musaka et al, and that routine experimentation as exemplified by the graph of Musaki would have provided parameters (such as flow rate) for the particular reaction chamber and gas used to produce the stress level desired. Lacking basis for determination, the claimed flow rates have little clear meaning. Note that Fluorosilicate glass is just amorphous silicon oxide with F, and that neither Nishiyama et al or Musaka appear to discuss whether their films are amorphous or crystalline, but the former are generally lower energy ~~temperatures~~ (temperatures) (ie lower and easier to form, as well as desirable for many uses in the semiconductor and electronics industry.

(14) The information disclosure is made of record and a copy of the PTO-1449 is enclosed Commonly seen values for internal stress for F-containing SiO_2 deposits, from plasma and other CVD depositions are noted with $2x10^8$ dyn/cm^2. (See Homma 5,288,518; col. 3, lines 42-45) being exemplary.

(15) The disclosure is objected to because of the following informalities: Concerning both applicant's and Musaka et al's negative stress values, it appears that the values may be shouldn't be negative, but just down an order of magnitude, otherwise the scales don't make sense, after all $0x10^9=0$, giving an incredibly broad jump from $0.5x10^9$ to $-0.5x10^9$. So are values really going from $+0.5 \times 10^9$ dyne/cm^2 to -1.25 dyne/cm^2 (Musaka et al, Fig. 13) or is this an artifact from somebodies attempt to simplify the numbering on the axis? In applicant's specification, Figures 3 and 4 appear equally erroneous, having positive and negative values all to the power of 10^9 and in dyne/cm^2. The examiner suspects that values that would make more sense are 0 is 0.1, -.5 is 0.05, -1.0 is .01, etc., but sees NO enablement for this in the specification.

Appropriate correction is required.

(16). Chebi et al is cited for its teachings that effect compressive stress in plasma deposited silicon fil on various parameters although they do not discuss the use of F in the reactants.

(17) Any inquiry concerning this communication should be directed to M. L. Padgett at telephone number (703) 308-2336 and fax no. (703) 305-3600.

M. Padgett/vr

10-02-97

MARIANNE PADGETT
PRIMARY EXAMINER
GROUP 1100

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 1 of 5 GROUP I	Attorney Docket No. AM-850/T08000	Serial No.: 08/691,983
	Applicant: Nowak et al.	
	Filing Date: 08/02/96	Group: 1112

Reference Designation 1997 U.S. PATENT DOCUMENTS (GROUP I)

Examiner Initial	Tab No.	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
AA	1	5,429,995	07/04/95	Nishiyama et al.	437	238	07/16/93
AB	2	5,399,529	03/21/95	Homma	437	195	05/26/93
AC	3	4,894,352	01/16/90	Lane et al.	437	238	10/26/88
AD	4	4,872,947	10/10/89	Wang et al.	156	643	10/26/88

FOREIGN PATENT DOCUMENTS

Examiner Initial	Tab No.	Document No.	Date	Country	Class	Sub-class	Translation (yes/no)
AE	5	WO 92/20833	11/26/92	PCT Weise	C23C	16/00	yes

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AF	6	Shapiro et al., "Dual Frequency Plasma CVD Fluorosilicate Glass Water Absorption And Stability", DUMIC Conference, Feb. 1995, pp. 118-123
AG	7	Takeishi et al., "Stabilizing Dielectric Constants of Fluorine-Doped-Si02 Films by N20-Plasma Annealing", DUMIC Conference, Feb. 1995, pp. 257-259.
AH	8	Carl et al., "The Effect of 0_2:C_2F_6 Ratios and Low Frequency Power On The Gap Fill Properties And Stability Of F-TEOS Films", DUMIC Conference, Feb. 1995, pp. 234-240.
AI	9	Musaka et al., "Single Step Gap Filling Technology For Subhalf Micron Metal Spacings On Plasma Enhanced TEOS/0_2 Chemical Vapor Deposition System", Extended Abstracts of the 1993 International Conference on Solid State Devices and Materials, Makuhari, 1993, pp. 510-512.

EXAMINER [signature] DATE CONSIDERED 9/20/97

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 2 of 5 GROUP I (CONTINUED)	Attorney Docket No. AM-850/T08000	Serial No.: 08/691,983
	Applicant: Nowak et al.	
	Filing Date: 08/02/96	Group: 1112

Reference Designation — U.S. PATENT DOCUMENTS, (GROUP II)

Examiner Initial	Tab No.	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub-class	Translation (yes/no)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

AJ	10	Robles et al., "Effects of RF Frequency and Deposition Rates on the Moisture Resistance of PECVD TEOS-Based Oxide Films", Vol. 92-1, ECS Extended Abstracts, p. 215, Abstract 129, May 1992.
AK	11	Galiano et al., "Stress-Temperature Behavior of Oxide Films Used For Intermetal Dielectric Applications", VMIC Conference, June 1992, pp. 100-106.

EXAMINER [signature] DATE CONSIDERED 9/24/97

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 3 of 5 GROUP II	Attorney Docket No. AM-850/T08000	Serial No.: 08/691,983
	Applicant: Nowak et al.	
	Filing Date: 08/02/96	Group: 1112

Reference Designation — U.S. PATENT DOCUMENTS (Group I)

Examiner Initial	Tab No.	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
AL	12	5,420,075	05/30/95	Homma et al.	437	195	04/14/93
AM	13	5,413,967	05/09/95	Matsuda et al.	437	235	05/03/94
AN	14	5,407,529	04/18/95	Homma	156	643	03/04/93
AO	15	5,403,630	04/04/95	Matsui et al.	427	583	10/27/93
AP	16	5,385,763	01/31/95	Okano et al.	427	572	03/01/94
AQ	17	5,319,247	06/07/94	Matsuura	257	760	10/25/91
AR	18	5,288,518	02/22/94	Homma	427	255	06/05/92
AS	19	5,334,552	08/02/94	Homma	437	195	11/24/92
AT	20	5,275,977	01/04/94	Otsubo et al.	437	235	03/14/91
AU	21	5,215,787	06/01/93	Homma	427	248.1	01/14/92
AV	22	5,156,881	10/20/92	Okano et al.	427	572	04/16/91
AW	23	5,013,691	05/07/91	Lory et al.	437	238	07/31/89
AX	24	4,851,370	07/25/89	Doklan et al.	437	225	12/28/87

FOREIGN PATENT DOCUMENTS

Examiner Initial	Tab. No.	Document No.	Date	Country	Class	Sub-class	Translation (yes/no)
AY	25	4-239750	08/27/92	JP Hoya	H01 L21	90	No (abstract only)
AZ	26	4-341568	11/27/92	JP Matsuda	C23C 16	40	No (abstract only)
BA	27	J6 1276-977-A	12/06/86	JP Canon KK	C23C 16	50	No (abstract only)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

BB	28	Fukada et al., "Preparation Of SiOF Films With Low Dielectric Constant By ECR Plasma CVD", DUMIC Conference, Feb. 1995, pp. 43-49.
BC	29	Qian et al., "High Density Plasma Deposition And Deep Submicron Gap Fill With Low Dielectric Constant SIOF Films", DUMIC Conference, Feb. 1995, pp. 50-56.

EXAMINER [signature] DATE CONSIDERED 9/25/97

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 4 of 5 GROUP II (CONTINUED)	Attorney Docket No. AM-850/T08000	Serial No.: 08/691,983
	Applicant: Nowak et al.	
	Filing Date: 08/02/96	Group: 1412

Reference Designation **U.S. PATENT DOCUMENTS, (GROUP II)**

Examiner Initial	Tab No.	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)

FOREIGN PATENT DOCUMENTS

		Document No.	Date	Country	Class	Sub-class	Translation (yes/no)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

BD	30	Matsuda et al., "Dual Frequency Plasma CVD Fluorosilicate Glass Deposition For 0.25 μm Interlevel Dielectrics", DUMIC Conference, Feb. 1995, pp. 22-28.
BE	31	Ravi K. Laxman, "Low ε Dielectrics: CVD Fluorinated Silicon Dioxides", Semiconductor International, May 1995, pp. 71-74.
BF	32	Hayasaka et al., "High-Quality And Low Dielectric Constant SiO_2 CVD Using High Density Plasma", Dry Process Symposium, Nov. 1994, pp. 163-168.
BG	33	Yu et al., "Step Coverage Study of Peteos Deposition For Intermetal Dielectric Applications", VMIC Conference, Jun. 1990, 166-172.
BH	34	Chang et al., "Frequency Effects and Properties of Plasma Deposited Fluorinated Silicon Nitride", J. Vac. Sci. Technol. B6 (2) 1988, pp. 524-532. Mar/Apr
BI	35	Webb et al., "Silicon Dioxide Films Produced By PECVD of TEOS and TMCTS", Proceedings of the Int. Symp. on Ultra Large Scale Integration Science and Technology, No. 9, 1989, Pennington, N.J., pp. 571-585.
BJ	36	Hoff et al., "Thermal Oxidation Of Silicon In An Afterglow Gas", (undated), Ctr. for Elect. Materials and Devices, Penn State Univ.

EXAMINER [signature] DATE CONSIDERED 9/20/97

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

FORM PTO-1449 (Modified) LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary) Page 5 of 5 GROUP III	Attorney Docket No. AM-850/T08000	Serial No.: 08/691,983
	Applicant: Nowak et al.	
	Filing Date: 08/02/96	Group: 1112

Reference Designation — U.S. PATENT DOCUMENTS (GROUP I)

Examiner Initial	Tab No.	Document No.	Date	Name	Class	Sub-class	Filing Date (If Appropriate)
BK	37	5,314,724	05/24/94	Tsukune et al.	427	489	12/19/91
BK	38	4,300,989	11/17/81	Chang	204	164	10/03/79

FOREIGN PATENT DOCUMENTS

Examiner Initial	Tab No.	Document No.	Date	Country	Class	Sub-class	Translation (yes/no)

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER [signature] DATE CONSIDERED 9/20/99

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

WHAT IS CLAIMED IS:

1. In a processing chamber, a method of depositing a layer having a predetermined intrinsic stress level over a substrate, said method including the steps of:

(a) distributing a halogen source to said processing chamber at a selected rate, said selected rate being chosen according to said predetermined stress level;

(b) introducing a process gas comprising silicon, oxygen and said halogen source into said chamber; and

(c) forming a plasma from said process gas to deposit said layer having said predetermined intrinsic stress level over said substrate.

2. The method of claim 1 wherein said predetermined stress level is a compressive stress level.

3. The method of claim 2 wherein said halogen source comprises a fluorine source.

4. The method of claim 3 wherein said fluorine source is selected from the group of: CF_4, C_2F_6, SiF_4 and TEFS.

5. The method of claim 4 wherein said silicon source comprises TEOS.

6. The method of claim 5 wherein said predetermined intrinsic stress level is between about -1.0×10^{-9} dynes/cm^2 and -0.5×10^{-9} dynes/cm^2.

7. The method of claim 6 wherein a dielectric constant of said layer is between about 3.8 to 4.1.

8. The method of claim 3 further comprising the steps of:

(d) repeatedly performing steps (a) through (c) to deposit a halogen-doped silicon oxide film on a plurality substrates;

(e) measuring the intrinsic stress of said deposited halogen-doped silicon oxide film on each of said plurality of substrates; and

(f) if said intrinsic stress of said deposited halogen-doped silicon oxide films is too high, increasing said selected rate at which said halogen source is introduced during deposition of a halogen-doped silicon oxide film over a subsequently processed substrate to lower the intrinsic stress of said subsequently deposited halogen-doped silicon oxide film, and if said intrinsic stress of said deposited halogen-doped silicon oxide films is too low, decreasing said selected rate at which said halogen source is introduced during deposition of a halogen-doped silicon oxide film over a subsequently processed substrate to increase the intrinsic stress of said subsequently deposited halogen-doped silicon oxide film.

9. The method of claim 3 wherein said selected rate is determined from a database of measured intrinsic stress levels of previously deposited films.

10. The method of claim 1 wherein said processing chamber comprises an HDP CVD chamber and said plasma is formed by application of RF power to a coil.

11. In a processing chamber surrounded at least in part by a coiled antenna, a method of depositing an insulating layer having a predetermined intrinsic stress level over a semiconductor substrate positioned in said chamber, said method including the steps of:

(a) distributing a fluorine-containing source to said processing chamber at a selected rate, said selected rate being chosen according to said predetermined stress level;

(b) introducing a process gas comprising silicon, oxygen and said fluorine-containing source into said chamber from a gas distribution manifold; and

(c) applying RF power to said coiled antenna to form an inductively coupled plasma having an ion density of at least 10^{11} ions/cm^3 from said

process gas thereby depositing a fluorosilicate glass (FSG) film of said predetermined stress level over said substrate.

12. The method of claim 11 wherein said fluorine source is selected from the group of: CF_4, C_2F_6, SiF_4 and TEFS.

13. The method of claim 12 wherein said silicon source comprises TEOS.

14. The method of claim 13 wherein said intrinsic stress level is between about $-1.0x10^{-9}$ dynes/cm^2 and $-0.5x10^{-9}$ dynes/cm^2.

15. The method of claim 14 wherein said fluorine source is introduced at a rate that is 20% or less of total gas flow into said chamber.

16. The method of claim 15 wherein said fluorine source is CF_4 and is introduced at a rate that is 10% or less of the total gas flow into said chamber.

17. An integrated circuit having an insulating layer formed by the process of claim 12.

identical to allowed claim #24

18. A substrate processing system comprising:

a housing for forming a vacuum chamber;

a substrate holder, located within said housing, for holding a substrate;

a gas delivery system configured to introduce a process gas into said vacuum chamber;

a plasma generation system configured to form a plasma from said process gas;

a controller for controlling said gas delivery system and said plasma generation system; and

a memory coupled to said controller comprising a computer readable medium having a computer readable program embodied therein for directing operation of said substrate processing system, said computer readable program comprising:

a first set of instructions for controlling said gas delivery system to introduce a process gas comprising silicon, oxygen, and a halogen source into said gas mixing area; and

a second set of instructions for controlling said plasma generation system to form a plasma from said gases by said first set of instructions to deposit a layer over said substrate;

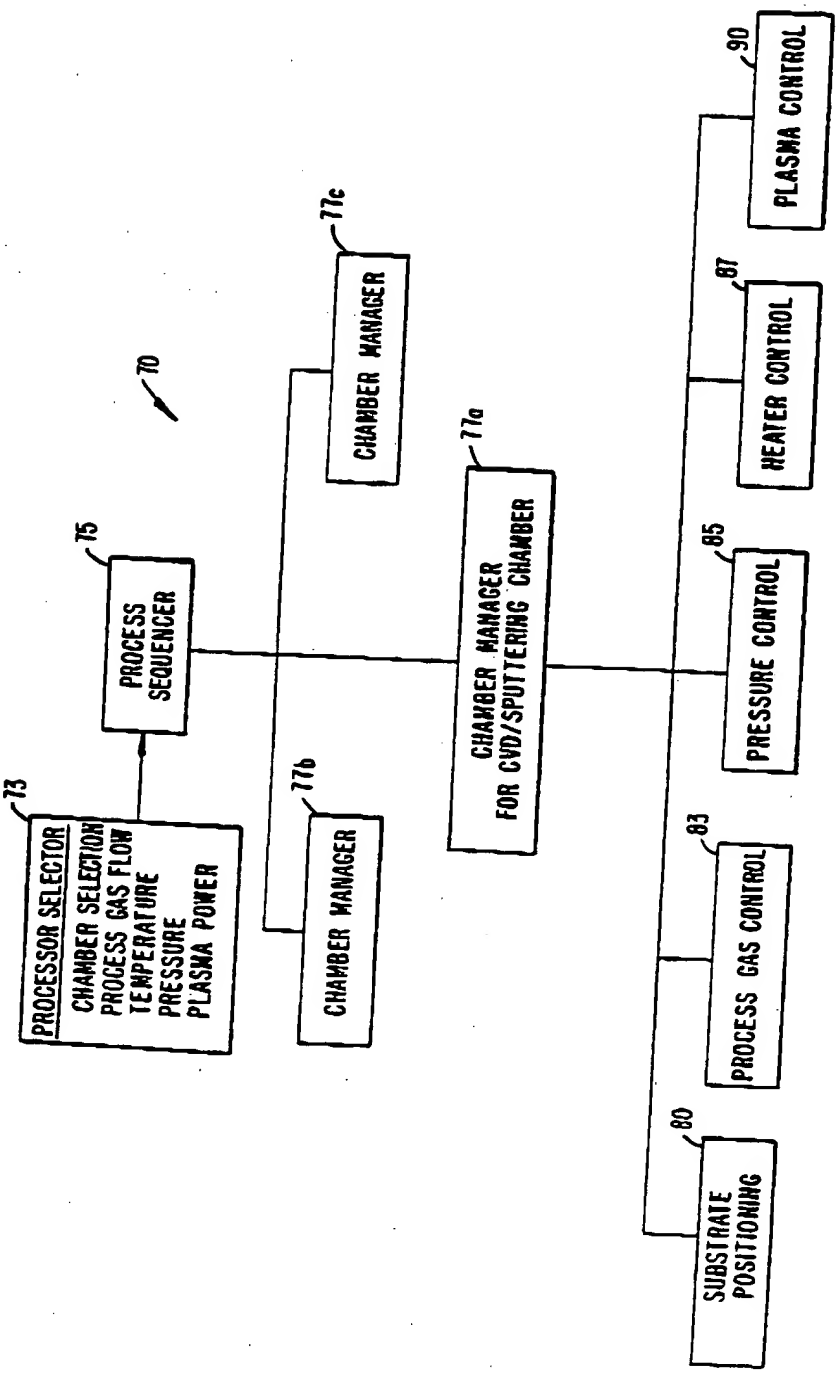
whereby said first set of instructions controls said gas delivery system to introduce said halogen source into said gas mixing area at a selected rate so that said deposited layer has a predetermined intrinsic stress level.

19. The substrate processing system of claim 18 wherein said plasma generation system comprises an inductive coil coupled to an RF power supply, said inductive coil at least partially surrounding said vacuum chamber; and

wherein said plasma formed by said plasma generation system has an ion density of at least 10^{11} ions/cm^3.

20. The substrate processing system of claim 19 wherein said first set of instructions controls said gas delivery system to introduce a fluorine source as said halogen source into said gas mixing area at a selected rate so that said deposited layer has a compressive stress level of between -1.0 to -0.5x10^9 dynes/cm^2.

21. The substrate processing system of claim 20 wherein said first set of instructions controls said gas delivery system to introduce said fluorine source into said chamber at a rate that is about 20% or less of the total gas flow into said chamber.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CHAMBER SELECTION
PROCESS GAS FLOW
TEMPERATURE
PRESSURE
PLASMA POWER
73
PROCESS SEQUENCER
75
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77c
CHAMBER MANAGER
77b
CHAMBER MANAGER
FOR CVD/SPUTTERING CHAMBER
77a
PRESSURE CONTROL
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HEATER CONTROL
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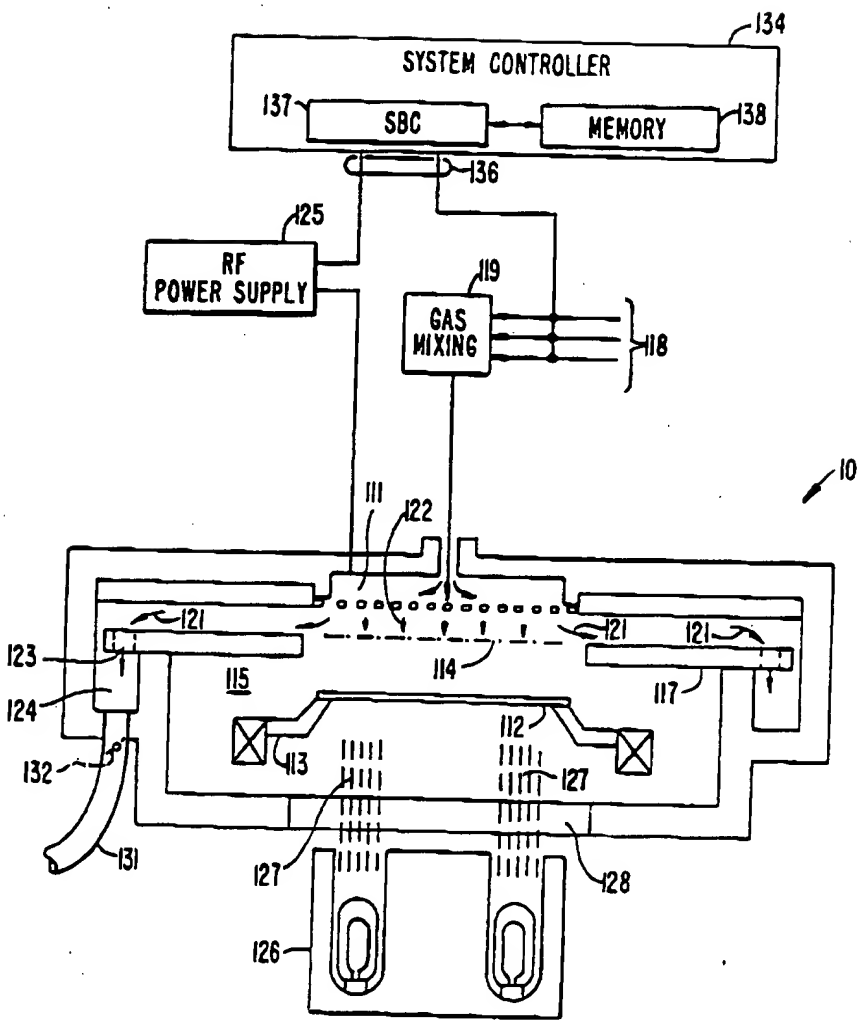
PLASMA CONTROL
90
PROCESS GAS CONTROL
83
SUBSTRATE POSITIONING
80

FIG. 1C.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MEMORY
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RF
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GAS
MIXING
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10
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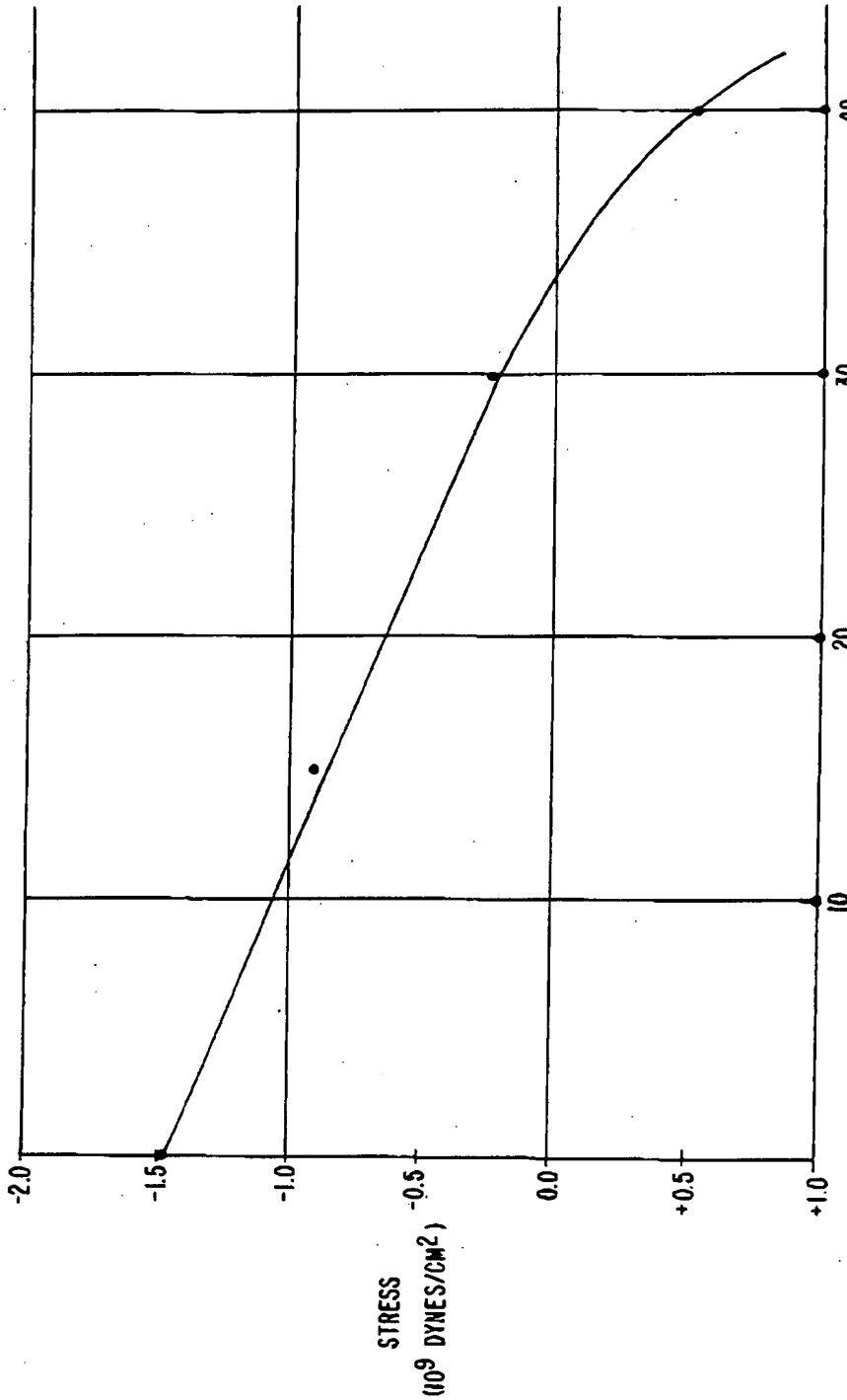
126

FIG. 2.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-1.0
-0.5
0.0
+0.5
+1.0
STRESS
(10^9 DYNES/CM^2)
10
20
30
40
CF_4 FLOW (SCCM)

FIG. 3.